ABSTRACT OF THE DISCLOSURE

A self aligned method of forming a semiconductor memory array of floating gate memory cells in a semiconductor substrate having a plurality of spaced apart isolation regions and active regions on the substrate substantially parallel to one another in the column direction, and an apparatus formed thereby. Floating gates are formed in each of the active regions. In the row direction, trenches are formed that include indentations or different widths. The trenches are filled with a conducting material to form blocks of the conducting material that constitute source regions with a first portion that is disposed adjacent to but insulated from the floating gate, and a second portion that this disposed over but insulated from the floating gate.